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TITLE: DATA TRANSFER CONTROL SYSTEM FOR INFORMATION
PROCESSOR
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ABSTRACT:

PURPOSE: To execute the retry even if a hard error is generated in a transfer line and transmitting and receiving registers by inverting all bits of transmitting data at the time when an error is detected, and also, reinverting all bits of receiving data.

CONSTITUTION: Data sent out of a transmitting side unit A is received by a receiving register 21 of a receiving side unit B, and when an error is detected, an error detecting circuit 22 informs the error to a receiving side data processing part 20 and a transmitting side data processing part 10 through an error detecting signal line 201 and (c), respectively. The transmitting side unit A executes an invert instruction, transmits that which is

obtained by
inverting all bits of transmitting data, and also, informs the
execution of the
invert instruction to the receiving side unit B through a control
signal line
(a). A software on the receiving side unit B inverts again all bits
of
receiving data, and this data after reinversion is used as receiving
data. In
such a way, even if a hard error is generated in a transfer line and
transmitting and receiving registers, the retry can be executed.

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